AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently amended) A circuit designing apparatus comprising:

a logic verification unit configured to ~~perform a logic verification by inputting~~ input a plurality of test vectors necessary for ~~the~~ a logic verification to a circuit description defining a structure and a specification of a circuit to be designed, ~~and comparing~~ to compare an output signal of the circuit description ~~and~~ with an expected value of the output signal, and ~~judging~~ to judge the validity of the circuit description in accordance with a result of the comparison;

a profile information generating unit configured to ~~store~~ detect information about a plurality of logic cones in the circuit description to be activated by the test vectors during the logic verification, [[in]] for each test vector, ~~as profile information~~ and to generate a profile information relating the test vector to the logic cones activated by the test vector;

a circuit changing unit configured to change the circuit description after the logic verification and to generate a changed circuit description;

a logic cone specifying unit configured to specify changed logic cones of the changed circuit description, based on a result of a formal verification; and

a test vector classifying unit configured to classify the test vectors into test vectors that activate the changed logic cones and test vectors that do not activate the

changed logic cones, ~~based on~~ by searching for the test vectors related to the changed logic cones in the profile information,

wherein the logic verification unit ~~performs the logic verification of the changed circuit description, based on~~ inputs the test vectors that activate the changed logic cones into the changed circuit description, compares an output signal of the changed circuit description with an expected value of the output signal, and judges the validity of the changed circuit description in accordance with a result of the comparison.

2. (Previously presented) The circuit designing apparatus of claim 1, further comprising:

a logic cone dividing unit configured to divide the circuit description into the logic cones; and

a formal verification unit configured to verify logic by formal technology using the circuit description and the changed circuit description.

3. (Currently amended) A circuit designing method comprising:

~~performing a logic verification by~~ inputting a plurality of test vectors necessary for ~~the~~ a logic verification to a circuit description defining a structure and a specification of a circuit to be designed; ~~and~~

comparing an output signal of the circuit description with ~~and~~ an expected value of the output signal; ~~and~~

judging the validity of the circuit description in accordance with a result of the comparison;

~~storing~~ detecting information about a plurality of logic cones in the circuit description to be activated by the test vectors during the logic verification, [[in]] for each test vector~~, as profile information~~;

generating a profile information relating the test vector to the logic cones activated by the test vector;

changing the circuit description after the logic verification;

generating a changed circuit description;

specifying changed logic cones of the changed circuit description based on a result of a formal verification;

classifying the test vectors into test vectors that activate the changed logic cones and test vectors that do not activate the changed logic cones, ~~based on~~ by searching for the test vectors related to the changed logic cones in the profile information; ~~and~~

~~performing a logic verification of the changed circuit description, based on~~ inputting the test vectors that activate the changed logic cones into the changed circuit description;

comparing an output signal of the changed circuit description with an expected value of the output signal; and

judging the validity of the changed circuit description in accordance with a result of the comparison.

4. (Previously presented) The circuit designing method of claim 3, further comprising:

dividing the circuit description into the logic cones; and

verifying logic by formal technology using the circuit description and the changed circuit description.

5. (Previously presented) The circuit designing method of claim 3, wherein the logic verification of the changed circuit description is executed by using preferentially the test vectors that activate the changed logic cones.

6. (Previously presented) The circuit designing method of claim 4, further comprising issuing a circuit description and processing circuit manufacture by using the circuit description.

7. (Previously presented) The circuit designing method of claim 5, further comprising issuing a circuit description and processing circuit design and manufacture by using the circuit description.

8. (Currently amended) A computer-readable recording medium storing a circuit designing program comprising and making a computer execute:

instructions configured to ~~perform a logic verification by inputting~~ input a plurality of test vectors necessary for the logic verification into a circuit description defining a structure and a specification of a circuit to be designed; ~~and comparing~~

instructions configured to compare an output signal of the circuit description with ~~and~~ an expected value of the output signal; ~~and judging~~

instructions configured to judge the validity of the circuit description in accordance with a result of the comparison;

instructions configured to ~~store~~ detect information about a plurality of logic cones in the circuit description to be activated by the test vectors during the logic verification, [[in]] for each test vector~~, as profile information~~;

instructions configured to generate a profile information relating the test vector to the logic cones activated by the test vector;

instructions configured to change the circuit description after the logic verification and to generate a changed circuit description;

instructions configured to specify changed logic cones of the changed circuit description based on a result of a formal verification;

instructions configured to classify the test vectors into test vectors that activate the changed logic cones and test vectors that do not activate the changed logic cones, ~~based on~~ by searching for the test vectors related to the changed logic cones in the profile information; ~~and~~

instructions configured to ~~perform a logic verification of the changed circuit description, based on~~ input the test vectors that activate the changed logic cones into the changed circuit description;

instructions configured to compare an output signal of the changed circuit description with an expected value of the output signal; and

instructions configured to judge the validity of the changed circuit description in accordance with a result of the comparison.

9. (Previously presented) The computer-readable recording medium storing a circuit designing program of claim 8, wherein the logic verification of the changed circuit description is executed by using preferentially the test vectors that activate the changed logic cones.

10. (Previously presented) The computer-readable recording medium storing a circuit designing program of claim 8, further comprising and making the computer execute:

instructions configured to output a circuit description,

wherein circuit manufacture is processed by using the circuit description.

11. (Previously presented) The computer-readable recording medium storing a circuit designing program of claim 8, further comprising and making the computer execute:

instructions configured to divide the circuit description into the logic cones; and

instructions configured to verify by formal technology using the circuit description and the changed circuit description.

12. (Previously presented) The circuit designing apparatus of claim 1, wherein the logic verification of the changed circuit description is executed by using preferentially the test vectors that activate the changed logic cones.

13. (Previously presented) The circuit designing apparatus of claim 1, wherein the second and subsequent logic verifications are executed by using only the test vectors that activate the changed logic cones.

14. (Previously presented) The circuit designing apparatus of claim 2, wherein the logic cone specifying unit specifies the changed logic cones on the basis of a result of the formal verification.

15. (Previously presented) The circuit designing method of claim 3, wherein the second and subsequent logic verifications are executed by using only the test vectors that activate the changed logic cones.

16. (Previously presented) The computer-readable recording medium storing a circuit designing program of claim 8, wherein the second and subsequent logic verifications are executed by using only the test vectors that activate the changed logic cones.